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EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/615,880	KAZI ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-21* is/are rejected.

7)☒ Claim(s) *22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to independent claims 1, 8, 15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5, 7 are rejected under 35 U.S.C. 103(a) as being obvious over Boccuzzi et al. (U.S. 5,786,725) in view of Chung et al. (U.S. 2004/0190655), Applicant's admitted prior art of the instant application (hereafter referred to as AAPA) and Huang et al. (U.S. 5,991,289).

With respect to claim 1, Boccuzzi et al., disclose: means for converting the input signal to in-phase and quadrature components (not shown, but see Fig. 1A, and Fig. 1B, DQPSK transmitter and receiver where it is understood that the I and Q signal are combined to be transmitted over the communication medium, and at the receiver I and Q signals are separated into I and Q signals); a differential demodulator to determine a demodulated phase by comparing the in-phase and quadrature components of the input signal with a first delayed, conjugated version of the in-phase and quadrature components of the input signal (see Fig. 2, differential detector, see column 2, lines 14-

16, 27-41); and a symbol mapping circuit to map the phase to an output symbol, comprising one or more bits of data (see column 1, table 1 and column 2, lines 42-49 for the symbol mapping based on the detected phase shift).

Boccuzzi et al., do not disclose: a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components of the input signal with a second delayed, conjugated version of the in-phase and quadrature components of the input signal; wherein the delay associated with the second delayed, conjugated version of the in-phase and quadrature components of the input signal is less than one symbol interval; a frequency correction circuit to correct the demodulated phase using the frequency offset into a corrected phase; a phase correction circuit to determine an absolute phase using the corrected phase;

In the same filed of endeavor, Chung et al., disclose: a frequency offset calculation circuit (see first sentence of paragraph [0004] and Fig. 1) to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components of the input signal with a second delayed, conjugated version of the in-phase and quadrature components of the input signal; wherein the delay associated with the second delayed, conjugated version of the in-phase and quadrature components of the input signal is one symbol interval; (see paragraph [0005] and Fig. 1 operation inside box 40 performed on symbols (the are the in-phase and quadrature components) and see estimation of $\Delta\theta$ phase rotation caused by the carrier offset).

Therefore at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Boccuzzi et al., so that it includes the frequency offset determination circuit of Chung et al., since phase errors introduced by carrier offset cause symbol phase rotation in differential demodulations (differential PSK, BPSK, QPSK) therefore the phase rotation caused by the frequency offset has to be known so that demodulation errors are avoided.

The AAPA discloses: a frequency correction circuit to correct the demodulated phase using the frequency offset into a corrected phase (see Fig. 2 of the instant application, adder 223 adding the phase error corresponding to the frequency offset to the phase determined from the differential demodulator); determining an absolute phase; and a symbol mapping circuit to map the absolute phase to an output symbol, comprising one or more bits of data [see last sentence of paragraph [0008]).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Boccuzzi and Chung, so that the phase rotation estimate (caused by the frequency (carrier) offset) is added to the phase determined by the differential demodulator so that a phase that is compensated for carrier offset is obtained. Also, it would have been obvious to a person of ordinary skill in the art to modify the system of Boccuzzi and Chung so that it includes a phase correction circuit that determines an absolute phase using the corrected phase so that it can be mapped to symbols and corresponding bits (AAPA, paragraph [0008]).

In the same field of endeavor (AFC, and DPQPSK receiver), Huang et al., disclose: a frequency offset calculation circuit (see column 5, lines 3-30 equation (1) Δf_R

is the carrier frequency offset, Fig. 4, see delay Tu, column 5, lines 41-46, Tu is approximately one-fifth of the overall symbol duration).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Boccuzzi, Chung, AAPA based on the teachings of Huang so that the second delay (used for a frequency offset estimation) is less than one symbol interval so that the frequency offset estimation is obtained with a minimal impact from multipath distortion (column 7, lines 15-33).

With respect to claim 2, Chung et al., discloses: removing noise and glitches caused by phase transients between symbols, see squaring operation of element 20 of Fig. 1, and second half of paragraph [0005] and all of paragraphs [0006]-[0007], where the squared phasor (that includes the frequency offset) that is insensitive to phase differences between successive modulated samples (understood to also include phase errors (transients) caused for example by non-ideal components), and see that the noise can be ignored).

With respect to claim 3, Boccuzzi et al., disclose: wherein the delay associated with the first delayed version of the in-phase and quadrature components of the input signal in the differential demodulator is approximately one symbol interval (column 2, lines 22-26, see that Ts is one symbol interval).

With respect to claim 5, all of the limitations of claim 1 are analyzed above in claim 1 and the AAPA discloses: further comprising an optimal sample calculation circuit

to determine an optimal sample to use to determine the demodulated phase and the frequency offset (see Fig. 2, elements 210, 212, 214, and the control of switches 208 and 216 see paragraphs [0008]-[0010] of the specification).

With respect to claim 7, all of the limitations of claim 7 are rejected above in claim 5, and claim 7 is rejected similarly to claim 2 above.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being obvious over Boccuzzi et. al. (U.S. 5,786,725) in view of Chung et. al. (U.S. 2004/0190655), Applicant's admitted prior art of the instant application (hereafter referred to as AAPA) and Huang et al. (U.S. 5,991,289) as applied to claim 1 above, and further in view of Legrand et al., (U.S. 6,674,822).

With respect to claim 6, neither Boccuzzi et al., or Chung, or AAPA or Huang disclose: wherein the optimal sample calculation circuit determines the optimal sample as the sample associated with a peak amplitude of the combined in-phase and quadrature components of each sample in each symbol interval.

In the same field of endeavor, Legrand et al., disclose: wherein the optimal sample calculation circuit determines the optimal sample as the sample associated with a peak amplitude each sample in each symbol interval (see column 1, lines 62-67, column 2, lines 7, column 3, lines 40-42, where the sample (and subsequently the sampling instant) with the maximum value is determined and keeps updating). At the time of the invention, it would have been obvious to a person skilled in the art at the

time of the invention, to use the teachings of Legrand in the system of Boccuzzi , to determine the optimal sample as the sample associated with a peak amplitude (maximum value) of the combined in-phase and quadrature components of each sample in each symbol interval. The benefit of using the teachings of Legrand et. al., in the system of the Boccuzzi (to perform best sample selection) include: limiting the number of computations and operating costs (see column 1, lines 49-51 of Legrand et. al.,)

5. Claims 1-3, 5 7-12, 14-16, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hendrickson et al., (U.S. 6,055,281) in view of Chung et al., (U.S. 2004/019655), Applicant's admitted prior art of the instant application (hereafter referred to as AAPA) and Huang et al. (U.S. 5,991,289).

With respect to claim 1, Hendrickson et al., disclose: means for converting the input signal to in-phase and quadrature components (see Fig. 2, and Fig. 3A showing details of block 210, see I and Q components out of mixers 306 and 308, column 7, lines 34-40, column 10, lines 33-39); a differential demodulator to determine a demodulated phase by comparing the in-phase and quadrature components of the input signal with a first delayed, conjugated version of the in-phase and quadrature components of the input signal (Fig. 2 block 212 Differential decoder, details of which are shown in Figure 4a, see column 16, lines 4-34); a symbol mapping circuit to map the absolute phase to an output symbol, comprising one or more bits of data (Fig. 2,

block I214, slicer, see column 17, lines 16-44, see table 2 where absolute values of the phase (Im) component are mapped into an output code).

Hendrickson et al., do not expressly teach: a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components of the input signal with a second delayed, conjugated version of the in-phase and quadrature components of the input signal; wherein the delay associated with the second delayed, conjugated version of the in-phase and quadrature components of the input signal is less than one symbol interval; a frequency correction circuit to correct the demodulated phase using the frequency offset into a corrected phase; a phase correction circuit to determine an absolute phase using the corrected phase;

In the same filed of endeavor, Chung et al., disclose: a frequency offset calculation circuit (see first sentence of paragraph [0004] and Fig. 1) to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components of the input signal with a second delayed, conjugated version of the in-phase and quadrature components of the input signal; wherein the delay associated with the second delayed, conjugated version of the in-phase and quadrature components of the input signal is one symbol interval (see paragraph [0005] and Fig. 1 operation inside box 40 performed on symbols (the are the in-phase and quadrature components) and see estimation of $\Delta\theta$ phase rotation caused by the carrier offset.

Therefore at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Hendrickson et. al., so that it includes the frequency offset determination circuit of Chung et. al., since phase errors introduced by carrier offset cause symbol rotation in differential demodulations (differential PSK, BPSK, QPSK) therefore the phase rotation caused by the frequency offset has to be known so that demodulation errors are avoided.

Applicant's admitted prior art discloses: a frequency correction circuit to correct the demodulated phase using the frequency offset into a corrected phase (Fig. 2, adder 223, adds the phase offset corresponding to the frequency offset to the phase out of the differential demodulator).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Hendrickson et al., and Chung et. al., based on the teachings of AAPA, so that the phase rotation caused by the frequency offset 9as taught by Chung) is added to the phase out of the differential decoder of Hendrickson et. al., so that the phase offset rotation is accounted for. With respect to the limitation, "a phase correction circuit to determine an absolute phase using the corrected phase;" see that in the system of Hendrickson et. al., modified by Chung and AAPA, the slicer takes an absolute value of the phase of the frequency-offset corrected phase.

In the same field of endeavor (AFC, and DPQPSK receiver), Huang et al., disclose: a frequency offset calculation circuit (see column 5, lines 3-30 equation (1) Δf_R is the carrier frequency offset, Fig. 4, see delay Tu, column 5, lines 41-46, Tu is approximately one-fifth of the overall symbol duration).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Hendrickson et al., Chung, AAPA based on the teachings of Huang so that the second delay (used for a frequency offset estimation) is less than one symbol interval so that the frequency offset estimation is obtained with a minimal impact from multipath distortion (column 7, lines 15-33).

With respect to claim 2, Chung et al., discloses: removing noise and glitches caused by phase transients between symbols, see squaring operation of element 20 of Fig. 1, and second half of paragraph [0005] and all of paragraphs [0006]-[0007], where the squared phasor (that includes the frequency offset) that is insensitive to phase differences between successive modulated samples (understood to also include phase errors (transients) caused for example by non-ideal components), and see that the noise can be ignored).

With respect to claim 3, Hendrickson et al., disclose: wherein the delay associated with the first delayed version of the in-phase and quadrature components of the input signal in the differential demodulator is approximately one symbol interval (see Fig. 4a, delay, column 16, lines 20-34 where in equation (10) is the product of symbol k and the conjugated version of symbol k-1, i.e. delay 403 has a duration of approximately one symbol interval).

With respect to claim 5, all of the limitations of claim 1 are analyzed above in claim 1 and the AAPA discloses: further comprising an optimal sample calculation circuit to determine an optimal sample to use to determine the demodulated phase and the frequency offset (see Fig. 2, elements 210, 212, 214, and the control of switches 208 and 216 see paragraphs [0008]-[0010] of the specification).

With respect to claim 7, all of the limitations of claim 7 are rejected above in claim 5, and claim 7 is rejected based on a rationale similar to the one used to reject claim 2 above.

With respect to claim 8,10 claims 8, 10 are rejected based on a rationale similar to the one used to reject claim 1 above. With respect to the limitations "digitizing the DPSK input signal" see Hendrickson et al., (column 10, line 33, 45-47,conversion of signal 159 to digital logic levels) and "filtering the I and Q components of the DSPK input signal to remove noise" see Fig. 3A, integrate and dump filters 310 of Hendrickson et. al.,)

With respect to claims 9, 11-12, 14 these claims are rejected based on a rationale similar to the one used to reject claims 3,2,5, 7 respectively above.

With respect to claims 15-19 these claims are rejected based on rationale similar to the one used to reject claims 8-12 respectively.

6. Claims 6, 13, 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hendrickson et al., (U.S. 6,055,281) in view of Chung et al., (U.S. 2004/019655), Applicant's admitted prior art of the instant application (hereafter referred to as AAPA), Huang et al. (U.S. 5,991,289) as applied to claims 1, 8, 15 and further in view of Legrand et al., (U.S. 6,674,822).

With respect to claim 6, neither Hendrickson et. al., or Chung, or AAPA or Huang et al. disclose: wherein the optimal sample calculation circuit determines the optimal sample as the sample associated with a peak amplitude of the combined in-phase and quadrature components of each sample in each symbol interval.

In the same field of endeavor, Legrand et. al., disclose: wherein the optimal sample calculation circuit determines the optimal sample as the sample associated with a peak amplitude each sample in each symbol interval (see column 1, lines 62-67, column 2, lines 7, column 3, lines 40-42, where the sample (and subsequently the sampling instant) with the maximum value is determined and keeps updating). At the time of the invention, it would have been obvious to a person skilled in the art at the time of the invention, to use the teachings of Legrand in the system of Hendrickson et. al.,, to determine the optimal sample as the sample associated with a peak amplitude (maximum value) of the combined in-phase and quadrature components of each sample in each symbol interval. The benefit of using the teachings of Legrand et al., in the system of the Hendrickson et. al., (to perform best sample selection) include: limiting the number of computations and operating costs (see column 1, lines 49-51 of Legrand et. al.,)

With respect to claims 13, 20 these claims are rejected based on a rationale similar to the one used to reject claim 6 above.

With respect to claim 21, Hendrickson et al., disclose: further comprising means for removing glitches caused by phase transients between symbols (see Fig.3A, integrated and dump filters for I and Q components).

Allowable Subject Matter

7. Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kim (U.S. 7,058,151)

Dick et. al., (U.S. 7,103,027)

Chung et. al., (U.S. 7,164,731)

Huang et al., (U.S. 5,991,289)

Tsuda et al., (U.S. 5,313,493)

LaBerge et al., (U.S. 5,142,287)

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is (571)272-5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SOPHIA VLAHOS/
Examiner, Art Unit 2611
6/11/2008

/Mohammad H Ghayour/
Supervisory Patent Examiner, Art Unit 2611